WHAT IS CLAIMED IS:

1. An automatic equalization circuit for receiving a digital training signal and a digital data signal and outputting a digital data signal equalized, comprising:

a first automatic equalization unit, to which said digital training signal and a digital data signal are supplied, for equalizing said digital data signal;

a memory for storing said digital training signal; and

a second automatic equalization unit coupled with said memory, for outputting an updating signal therefrom, the equalization characteristic of which is updated on the basis of said digital training signal from said memory, wherein said updating signal from said second automatic equalization unit is supplied to said first automatic equalization unit, so that the equalization characteristic of said first automatic equalization unit is updated.

2. An automatic equalization circuit according to Claim 1, wherein said second automatic equalization unit includes an equalizer having a configuration substantially the same as an equalizer of said first automatic equalization unit.

3. An automatic equalization circuit according to Claim 1, wherein, said digital training signal and digital data signal are supplied to said first automatic equalization unit through a delay circuit,

the delay time of which is predetermined.

4. An automatic equalization circuit according to Claim 1, wherein said digital training signal is read out from said memory in accordance with a processing rate of said second automatic equalization unit.

5. An automatic equalization circuit according to claim 1, wherein said first automatic equalization unit receives said digital training signal and said digital data signal, alternately.

6. An automatic equalization circuit according to Claim 1, wherein said memory is a FIFO memory.

7. An automatic equalization circuit according to Claim 1, wherein said memory is a RAM.

8. A receiver circuit for reproducing a training signal and a data signal modulated by a digital multilevel modulation system, comprising:

a signal processing unit, to which said training signal and a data signal are supplied, for producting a digital training signal and a digital data signal;

a first automatic equalization unit coupled with said signal processing unit, for equalizing said digital data signal, and outputting a digital data signal equalized;

a memory coupled with said signal processing unit, for storing said digital training signal; and

a second automatic equalization unit coupled

with said memory, for outputting an updating signal therefrom, the equalization characteristic of which is updated on the basis of said digital training signal from said memory, wherein said updating signal from said second automatic equalization unit is supplied to said first automatic equalization unit, so that the equalization characteristic of said first automatic equalization unit is updated.

9. A receiver circuit according to Claim 8, wherein said second automatic equalization unit includes an equalizer having a configuration substantially the same as an equalizer of said first automatic equalization unit.

10. A receiver circuit according to Claim 8, further comprising a delay circuit coupled between said signal processing unit and said first automatic equalization unit, the delay time of which is predetermined.

11. A receiver circuit according to Claim 8, wherein said first automatic equalization unit receives said digital training signal and said digital data signal, alternately.

12. A receiver circuit according to Claim 8, wherein said digital training signal is read out from said memory in accordance with a processing rate of said second automatic equalization unit.

13. A receiver circuit according to Claim 8, wherein said memory is a FIFO memory.

14. A receiver circuit according to Claim 8, wherein said memory is a RAM.